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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/338,473	06/22/1999	YOUNG-CHUN KIM	8836-116-(IB	1425

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EXAMINER
PATEL, GAUTAM

ART UNIT	PAPER NUMBER
2651	6

DATE MAILED: 11/30/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/338,473	Kim et al.
Examiner	**Art Unit**
Gautam R. Patel	2651

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 1, 2001*

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-25* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☒ Claim(s) *9-25* is/are allowed.

6) ☒ Claim(s) *1-8* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

Response to Amendment

1. This is in response to amendment filed on 10-01-01 (Paper # 5).

2. Claims 1-25 remain for examination.

3. Applicant's arguments regarding rejection of claims 2-25 under 35 U.S.C. § 112 first and second paragraph have been fully considered and rejection of claims 2-25 under 35 U.S.C. 112 first and second paragraph has been **withdrawn**.

Claim Rejections - 35 U.S.C. § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

5. Claims 1-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kai et al., US. patent 5,287,309 (hereafter Kai) in view of Koppala (US. patent 6,67,488) (hereafter Koppala).

As to claim 1, Kai discloses the invention as claimed [see Figs. 1-5] including a stack storage, a stack pointer circuit and a control signal comprising:

a stack storage [fig. 2, unit 5] comprising a plurality of banks [fig. 2, units 10 and 11] each comprising storage locations [col. 4, lines 14-20 and 27-39];

a stack pointer circuit [fig. 2, unit 6] comprising a bank pointer for each bank [(SPM + SPL), $\overline{SPL}$], wherein each bank pointer points to a storage location of a corresponding bank, and wherein the stack pointer circuit is responsive to at least one control signal [fig. 2, unit 7][col. 5, lines 45-62] [col. 4, line 58 to col. 5, line 16];

Kai disclose all of the above elements. Kai also discloses that a single pointer {SPM] can perform two operations simultaneously [PUSH and POP], and one signal is for pushing [or inserting] a word on the stack. Kai does not disclose that this single pointer can also POP [remove] two-word item form the stack, but Kai suggest that variation of the simultaneous POP and PUSH can be implemented, and this can be done by determination of the even and odd addresses and simple mathematical transformation [col. 2, lines 18-28; Kai]. However Koppala clearly discloses that control signal can be used for inserting a two-word or multi-word item into said stack storage and removing a two-word item from adjacent locations at a given time [col. 24, lines 21-40]. One of ordinary skill in the art would have realized that it is possible to execute two POP operation [or removing two-word item form the stack] instead of one PUSH and one POP operation in the system of Kai by simply transforming the logic as suggested by Kai. Also Koppala clearly discloses that "The most common stack manipulation for stack based computing system is to pop the two words from a stack and to push a data word onto the top of the stack" [col. 24, lines 29-32]. It would have been obvious to one of ordinary skill in the art at the time invention to have provided the a circuit of Kai with capability to remove two-word item form the stack storage as taught and suggested by Koppala, because it would have provided to a mechanism to execute the either two PUSH or two POP operation on the stack, thus making the stack operation much faster. NOTE: Two separate banks [fig. 2, units 10 and 11] and pointers going to them causes multi-word pop or push operation.

6. As to claim 2, Kai discloses:

a stack storage [fig. 2, unit 5] comprising a plurality of banks each comprising storage locations for storing stack items [fig. 2, units 10 and 11] [col. 4, lines 14-20 and 27-39];

a plurality of stack pointers [SPM, SPL etc.], the stack pointers comprising a main stack pointer [fig. 2, unit 6] for pointing to a top location of the stack storage and a bank pointer for each bank, wherein each bank pointer points to a storage location of a corresponding bank based on the content of the main stack pointer [fig. 2, unit 6] [col. 4, lines 58-63]; and

a controller [fig. 2, units 7, 8 and 9] responsive to at least one of the decoding signals for inserting bank address data into at least two bank pointers to perform multi-word push or multi-word pop operation [col. 4, lines 21-63];

NOTE: Two separate banks [fig. 2, units 10 and 11] and pointers going to them causes multi-word pop or push operation.

7. As to claim 3, Kai discloses:

each location of said stack storage is configured for storing a one-word item [inherently one-word is stored in stack memory].

8. As to claim 4, Kai discloses:

a two word item is one of inserted into and removed from two adjacent locations at a given time [col. 24, lines 21-40].

9. As to claim 5, Koppala discloses:

said stack storage control circuit increases and decreases the content of said stack pointer by one when the decoding signals indicate a one-word stack operation; and wherein said stack storage control circuit increases and decreases the content of

said stack pointer by two when the decoding signals indicate a two-word stack operation [col. 24, lines 21-61].

10. As to claim 6, Kai discloses:

a stack storage [fig. 2, unit 5] including a plurality of locations, wherein each of the locations of said stack storage is assigned to one of a first [fig. 2, unit 10] and a second bank [fig. 2, unit 11] [col. 4, lines 27-39];

a main stack pointer [fig. 2, unit 6, SPM] for pointing to a location of said stack storage [col. 4, lines 59-63];

a first bank stack pointer [fig. 2, unit SPL] for pointing to a location assigned to said first bank [fig. 2, unit 10] [col. 5, lines 17-62];

a second bank stack pointer [fig. 2, unit SPL bar] for pointing to a location assigned to said second bank [fig. 2, unit 11] [col. 5, lines 17-62];

an instruction decoder [inherently present] for decoding a stack-based instruction and generating a plurality of decoding signals [col. 4, lines 14-20]; and

a stack pointer control logic circuit [fig. 2, units 7, 8 and 9] for controlling said first and second bank stack pointers in response to at least one of the decoding signals to insert bank address data into the first and second bank stack pointers based on the content of the main stack pointer to perform a multi-word push or multi-word pop operation [col. 4, lines 21-63];

11. As to claim 7 Kai discloses:

said stack storage comprises 2 n+1 locations, n being a positive integer, and wherein the first bank and the second bank each include 2 n locations [col. 4, lines 46-57].

12. As to claim 8 Kai discloses:

one of the first and second banks includes locations with addresses having a least significant bit of logic `0' and the other of the first and second banks includes locations with addresses having a least significant bit of logic ` 1' [col. 4, lines 40-45].

Kai and Koppala were cited as prior art references in paper no. 4, mailed 7-2-01.

13. Applicant's arguments filed on 10-01-01 (Paper # 5) have been fully considered but they are not deemed to be persuasive for the following reasons.

14. In the REMARKS, the Applicant argues as follows:

A) That: "there is nothing in Kai that discloses or suggests the claimed feature of a stack pointer circuit "responsive to at least one control signal to insert bank address in at least two banks pointers to perform a multi-word push or multi-word pop operation" as recited in claim 1." [page 10, para. 2; REMARKS].

FIRST: See new rejection supra.

SECOND: Figure 2, in Kai clearly discloses a control signal. Unit 7 has control signal C coming into it which affects BOTH pointers SPM and SPL. These pointers go to BOTH banks 10 and 11. This causes multi-word [one word in bank 10 and another word in bank 11] push or pop operation, exactly as claimed.

B) That: "Kai does not disclose or suggest a stack "bank pointer" associated with each stack "bank", as essentially claimed in claim 1. [page 11, para. 1; REMARKS].

Kai clearly discloses a pointer going to both banks see fig. 2, pointers SPM, SPL, SPL_bar etc.].

Allowable Subject Matter

15. Claims 9-25 are allowed over the prior art of record.

16. **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

Contact information

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is (703) 308-7940. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.

The appropriate fax number for the organization (Group 2650) where this application or proceeding is assigned is (703) 872-9314.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. David Hudspeth, can be reached on (703) 308-4825.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-4700 or the group Customer Service section whose telephone number is (703) 306-0377.

RICHARD L. ELLIS
PRIMARY EXAMINER

Gautam R. Patel
Patent Examiner
Group Art Unit 2651

November 27, 2001